#17 Reply Brief 12-19-03 ars

Docket No.: 57454-257 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Customer Number: 20277
Fukashi MORISHITA	:	Confirmation Number: 7366
Serial No.: 09/987,566	:	Group Art Unit: 2816
Filed: November 15, 2001	:	Examiner: Terry D. Cunningham

For: INTERNAL POWER SUPPLY VOLTAGE GENERATION CIRCUIT THAT CAN SUPPRESS REDUCTION IN INTERNAL POWER SUPPLY VOLTAGE IN NEIGHBORHOOD OF LOWER LIMIT REGION OF EXTERNAL POWER SUPPLY VOLTAGE

REPLY BRIEF

Mail Stop Reply Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Reply Brief is submitted in response to the Examiner's Answer mailed October 3, 2003.

Claims 19 and 20 are pending. These claims stand rejected under 35 U.S.C. § 102(e) as being anticipated by Bion et al. (5,862,091).

Claim 19 recites level detection circuitry for detecting a difference between a first voltage and a second voltage. The level detection circuitry comprises a differential stage, including a first insulated gate transistor and a second insulated gate transistor.

The first insulated gate transistor receives a power supply voltage as the first voltage at a gate thereof and has a first conduction node, and a second conduction node for outputting a difference signal. The second insulated gate transistor receives a reference voltage as the second voltage at a gate

thereof and having a first conduction node connected to the first conduction node of the first insulated gate transistor. The second insulated gate transistor has a current supply ability different from a current supply ability of the first insulated gate transistor under a condition of the same gate voltage. The difference signal corresponds to a difference between the first and second voltages. The reference voltage determines a voltage level of an internal voltage generated from the power supply voltage.

Also, the level detection circuitry comprises:

- operation current supply circuitry for supplying an operation current to the first and second insulated gate transistors, the operation current supply circuitry comprising a current mirror coupled to the first and second insulated gate transistors for supplying current to the first and second insulated gate transistors; and

- a buffer circuit for buffering the difference signal for generating a binary level detection signal indicating whether the first voltage is higher than the second voltage.

In the Appeal Brief, Appellant argued that the reference does not disclose the claimed differential stage producing a difference signal corresponding to a difference between a power supply voltage and a reference voltage that determines a voltage level of an internal voltage generated from the power supply voltage, as claim 19 requires. In particular, Appellant submitted that the output of the comparator 37 of Bion does not produce a difference signal corresponding to a difference between the power supply voltage Vcc and the reference voltage produced from the power supply voltage Vcc.

In response, the Examiner takes the position that claim 19 does not recite that the difference signal corresponds to a difference between the power supply voltage Vcc and the reference voltage Vcc. The Examiner believes that claim 19 states only that difference signal corresponds to a difference between the first and second voltages.

It is noted that the Examiner erroneously identified the reference voltage of Bion as voltage

Vcc. The Appeal Brief indicates that the output of the comparator 37 of Bion does not produce a difference signal corresponding to a difference between the power supply voltage Vcc and the **reference voltage produced from the power supply voltage Vcc**.

In addition, the Examiner asserts that the claim 19 states only that the first insulated gate transistor receives a power supply voltage, and that the second insulated gate transistor receives a reference voltage.

It is respectfully submitted that the Examiner's interpretation of the claim language is not accurate. Claim 19 recites that the power supply voltage is received as the first voltage, and the reference voltage is received as the second voltage. Accordingly, the difference signal corresponding to a difference between the first and second voltages also corresponds to a difference between the power supply voltage and the reference voltage.

Moreover, the claim recites that the reference voltage determines a voltage level of an internal voltage generated from the power supply voltage. Accordingly, claim 19 requires the difference signal to correspond to a difference between a power supply voltage and a reference voltage that determines a voltage level of an internal voltage generated from the power supply voltage.

It appears that the Examiner recognizes that Bion et al. does not disclose the claimed differential stage producing a difference signal corresponding to a difference between a power supply voltage and a reference voltage that determines a voltage level of an internal voltage generated from the power supply voltage, as claim 19 requires.

Further, it appears that the Examiner misunderstood Appellant's arguments in the second and fourth full paragraphs of page 7. Appellant did not argue that the comparator of Bion performs no comparison. Instead, Appellant demonstrated that if the reference voltage at the non-inverting input corresponded to the internal voltage, as the Examiner contends, then both inputs of the comparator 37

would receive the same internal voltage, and the comparison with the power supply voltage would not be performed.

Also, Appellant argued that Bion et al. does not disclose a detection signal indicating whether the power supply voltage is higher than the reference voltage that determines the internal voltage generated from the power supply voltage. The Examiner takes the position that this limitation is not found in the claim, because the claim recites a detection signal indicating whether the first voltage is higher than the second voltage.

However, as discussed above, claim 19 recites that the power supply voltage is received as the first voltage, and the reference voltage is received as the second voltage. Therefore, the claim requires the detection signal to indicate whether the power supply voltage is higher than the reference voltage that determines the internal voltage generated from the power supply voltage.

Further, the Examiner takes the position that "nowhere does the claim recite that the circuit is always receiving 'power supply voltage as the first voltage'" or that the circuit is always receiving "reference voltage as the second voltage." The Examiner concludes that "the circuit [of Bion] receives the power supply voltage Vcc when transistor 36 is on, meeting the claim language, and the circuit receives the voltage at the drain transistor 38, meeting the claim language."

This Examiner's position is respectfully traversed. Anticipation, under 35 U.S.C. § 102, requires that each element of a claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. Accordingly, it is irrelevant whether or not the power supply and reference voltages are always received as the first and second voltages.

It is respectfully submitted that the Bion et al. arrangement never produces a difference signal corresponding to a difference between a power supply voltage and a reference voltage that determines a voltage level of an internal voltage generated from the power supply voltage, as claim 19 requires.

Further, this arrangement never produces a detection signal indicating whether the power supply voltage is higher than the reference voltage that determines the internal voltage generated from the power supply voltage, as claim 19 requires.

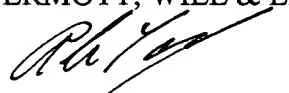
Accordingly, Bion et al. does not anticipate the invention recited in claim 19 within the meaning of 35 U.S.C. § 102.

For the above reasons, Appellant respectfully contends that the rejection of claims 19 and 20 as being anticipated under 35 U.S.C. § 102 is improper as the Examiner has not met the burden of establishing a *prima facie* case of anticipation. Reversal of the rejection in this appeal is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



Alexander V. Yampolsky
Registration No. 36,324

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 SAB:AVY:
Facsimile: (202) 756-8087
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